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| Industrial Placement Preliminary Report |
| --Hardware Regression Test |
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| **HAO DING (HD1812)** |
| **5/18/2015** |

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**Executive Summary**

The report provides an overview about the major project with TTP Meteor Ltd. Content includes background introduction, project outline, and technical details and progress. Comparison with other approaches and a web link to the latest project timeline can be found in appendix. The report is written at the early stage of placement.

This project is about including hardware components in regression test, aiming at improving working efficiency of hardware development in TTP Meteor. The output of final deliverables should provide sufficient information to convince users that no additional error is introduced after code modification, or to shows the reasons of test failures. The main idea of this project is sending hardware outputs back to PC for evaluation and analysis. Technical skills involved include PCB design, hardware development (VHDL) and software development (C#).

This project is based in The Technology Partnership (TTP) Group, which is a technology and product development company in Cambridge. This placement is with TTP Meteor, which is part of TTP group and specialized in industrial print head driver systems.

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**1. Introduction**

**1.1 Company Overview**

Since the foundation of TTP twenty-five years ago, TTP has been playing a pioneering role in a broad range of areas, including drug discovery, laboratory instrumentation, digital printing, etc. Now TTP is a team of over 300 engineers and scientists, working closely to invent and develop new products and processes. Today the enterprise has grown into TTP Group and new companies have been created inside this group.

TTP Meteor is one of them. Currently TTP Meteor has fourteen engineers working on technical development and several salesmen located in Europe, Asia and America. TTP Meteor has evolved and becomes a separate company this year, but still responsible for TTP Group. In recent years, TTP Meteor is growing and expanding rapidly with an increase of over 100% in revenue last year.

**1.2 Project Background**

Meteor particularly focuses on print head driver systems, including both software and hardware. Meteor driver systems are designed with high reliability and flexibility and it easily adapts to new print heads. The typical Meteor architecture consists of three layers: a Meteor head driver card (HDC), a print controller card (PCC), and PC applications.

**PC**

**Print Controller Card (PCC)**

**Head Drive Card (HDC)**

**Print Head**

**Figure 1.** TheTypical Meteor Hardware Architecture. (Arrow indicates major signal flow)

Figure 1 shows the most common Meteor driver architecture. HDC is the FPGA board to drive the specific print head. PCC is a FPGA board which controls various types of HDCs, typically controlling 8 HDCs. Meteor Architecture is a flexible and cost effective solution, which can be easily re-configured to meet changing and evolving requirements in printing industry. Hence, our clients are able to switch their options between different print head options with low cost.

My background project is based on the Meteor architecture and aims at improving the reliability and working efficiency of hardware development process by including hardware in regression tests.

Due to the fast-changing demand of printing industry, Meteor has often seen the case that the new driver system required to develop can use existing software and PCC but a new HDC, since some print heads follow similar design principles. It shows the major advantage of Meteor Hardware Architecture which reduces design complexity and allows engineers to provide reliable solutions within limited time with low cost. But it also brings the risk that each modification on hardware code, either due to code development or debugging, might lead to unpredicted result on other HDC using the same driver. Therefore, complete regression tests on all affected print heads are performed before each release to ensure the adaptability of the driver system. Regression tests require manual operations that are complicated and time-consuming, such as replacing print head, investigating analogue signals and comparing print result using naked eyes.

Instead of printing with different manually, my project provides a time-efficient and reliable alternative, shown in figure 2.

**Figure 2.** Hardware regression test signal flow diagram. (Arrow indicates major signal flow)

**PCC**

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**PC**

Wiring the signals from HDC back to PC side allows complicated testing process to be performed in software. Result about printing correctness can be generated by comparing actual driving signals with correct driving signals. As long as incoming signals provides sufficient information, generated result is reliable and same image will be printed with an operative print head. The idea is reasonably straight-forward while the challenge of this project will be how to make the final solution most convenient and practical to use in hardware development.

**2. Project Overview**

**2.1 Technical Details**

There are many possible approaches to carry out this project and probably most of them will succeed. After considering result expectation, project complexity, cost, etc, using an existing FPGA board (PCC-X) to bridge computer and HDC outputs is decided, mainly due to its convenience in practical operation.

**Typical Meteor Driver Architecture**

**PC**

**PCC**

**PCC-X (FPGA)**

**HDC**

**FX2 Interface**

**HDC Testboard**

**Adaptor**

**Hardware Regressive Test Architecture**

**Figure 3.** Working principles of hardware regressive test architecture

Figure 3 illustrates the architecture of hardware regression test. Testboard is essentially an existing modifiable board to check HDC is manufactured correctly. So all useful signals can be found on testboard. Note that the HDC and testboard marked in the red box will be replaced to test different print heads.

Following the project procedure above, technical work involved in my project is mainly composed of three main parts.

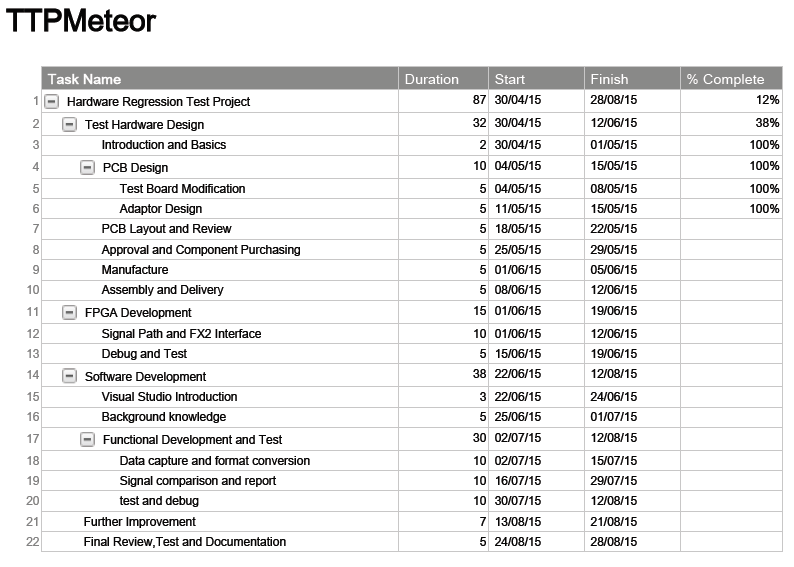
First of all, Adaptor board design is expected, including schematics, PCB layout using Altium and component selection. Before PCB board being sent to manufacture, it is important to ensure its adaptability and reliability. It is desired that adaptor board is able to collect signals from seven most popular HDC board, with a maximum of 32 digital and 32 analogue signals. A suitable mechanism is also required to transfer signals with high speed and low noise. Several HDC testboards also desire modification in order to connect to adaptor.

Secondly, PCC-X is a controller card with connectors and FX2 chip, which can be used for data transmission. I will write FPGA code in Quartus to communicate with PC and control adaptor board to perform signal sampling and data transfer. The challenge is to gather sufficient information from maximum of 64 signals, while the peak frequency of analogue signal is 10 MHz. A reasonable data format might improve the transmission speed significantly.

Thirdly, PC application is the user interface which communicates with PCC-X, sending commands and receiving data through FX2 interface. Then signals will be compared with database and a reliable report will be generated for user. PC application will be written in Visual Studio using C# as main language.

Another possible approach is using equipments provided by National Instruments. However, after careful research and comparison, this plan is eventually abandoned. Details are included in **Appendix I**.

**2.2 Timeline and project plan**

After two weeks of background learning and preparation, I listed expected tasks and workloads, and made the following timeline.

**Figure 4.** Project Timeline

Please find the link in **Appendix II** for latest project plan and weekly updated progress. Notice that this project plan has provided sufficient time on each single task including learning and familiarizing software, actual progress is expected to be faster than plan. Also, this timeline terminates two weeks before end of placement. This arrangement is to comprise any contingency during the placement, such as exam, unexpected technical problem that causes project delay.

**2.3 Project Progress**

As shown in the timeline above, currently this project is at the stage that PCB design and layout in Altium are finished and in peer review while FPGA development is has just begun.

**2.3.1 PCB Design**

**Adaptor Board**

Adaptor PCB is controlled by FPGA and it contains sufficient number of digital and analogue channels for various print heads.

**32-bit Digital Signals**

**Connector1**

**PCC-X (FPGA)**

**8-bit Digital**

**1 Analogue Signal**

**32 Analogue Signals**

**Connector2**

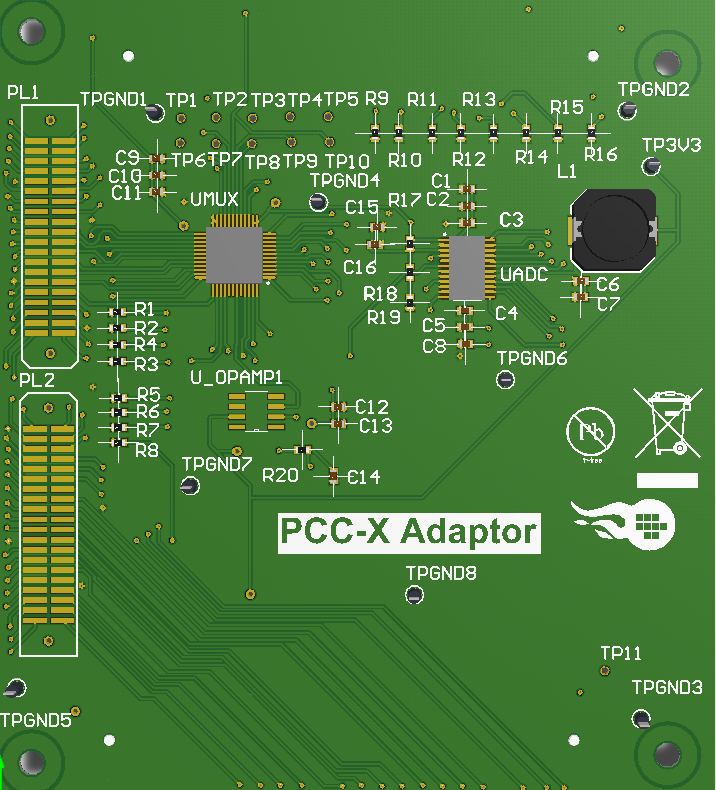
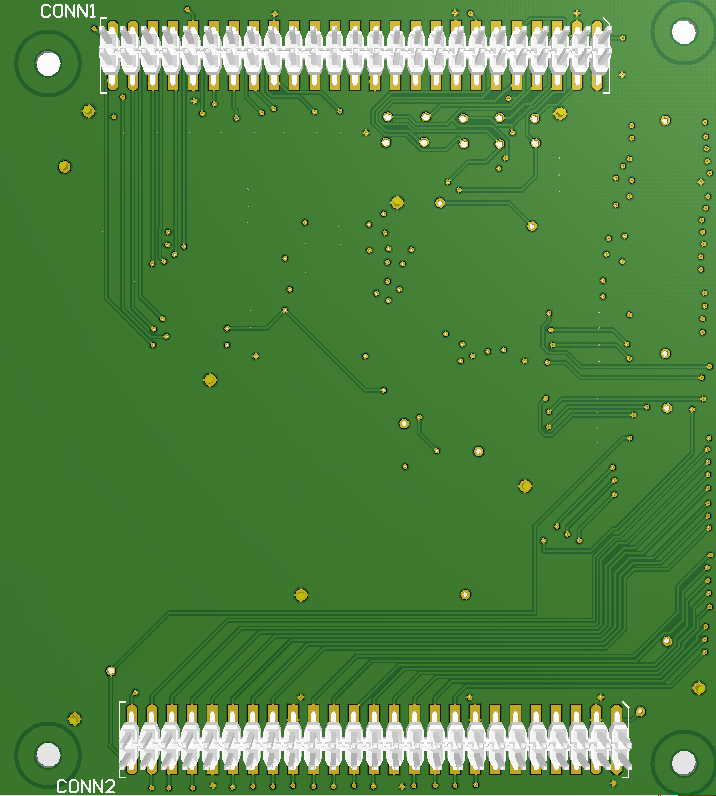
**ADC**

**MUX**

**Figure 5.** Adaptor Structure

Figure 5 shows a general structure of adaptor PCB board. Signals output from HDC consist of digital signals, such as image data, clock, and analogue signals such as trigger waveforms, sensor signals, etc. All digital signals will be collected directly and simultaneously by FPGA, while some analogue signals cannot be directly passed to FPGA due to high voltage and high frequency. Some print heads using specific piezo technology require high voltage waveform, up to 130 volts, to eject ink drops to reach target distance. Most of waveforms are generated through DAC with conversion rate of 10 Msps. Therefore, a high-speed ADC with conversion rate above 20 Msps is desired with suitable potential divider design to reduce input waveform to meet voltage rating. Due to the limitation of board size, it is difficult and unnecessary to collect all analogue signals at the same time. One sample from each channel is able to provide sufficient information about waveform shape if it is a waveform signal or voltage level if it is a constant voltage supply.

To reduce the influence of noise and improve the adaptor board performance, there are some other approaches to consider. For example, inserting ground level between fast-varying signal channels is necessary to prevent crosstalk between them. In addition, an active low pass filter is inserted between multiplexer and ADC to remove high frequency noise above 10 MHz. Other issues like mounting point, test point, and capacitor bypassing are also considered for the practical use of the board.



**Figure 6.** 3D simulation of adaptor PCB top layer (left), bottom layer (right)

Figure 6 is the simulated PCB for adaptor board. Analogue signals from PL1 pass through multiplexer, low-pass filter, ADC and then transferred to PCC-X through CONN1. Digital signals from PL2 are passed directly to PCC-X through CONN1.

**Testboards**

Modifications on existing testboard are performed including adding connectors and potential divider stages in order to match the PCC-X adaptor. Most modifications are straight-forward and will not be discussed in detail in this report.

**2.3.2 FPGA development**

FPGA development is at an early stage that a design proposal has been approved by my supervisor and the implementation is in progress. The following diagram illustrates a simplified design outline of FPGA development.

**FIFO**

**Packaging Block**

**8-bit Analogue Signal (After ADC)**

**32-bit Digital Signals**

**Control Block**

**Trigger Generator**

**FX2 Fast Databus**

**CPU Interface**

**Figure 7.** Simplified Design Outline

The main task of FPGA program is to sample all necessary signals, which are packaged and sent to PC via FX2 high speed databus. In order to obtain distinguishable and well-synchronised data, each signal channel is sampled for a finite period, depending on actual firing frequency, and each signal packet is added with a header, indicating data source and starting point. Considering practical problems during printing, the trigger signal which shows the beginning of each firing period is generated from incoming digital signals which contain most useful information about printing process. Note that this design is still in development and waiting to be tested for feasibility and efficiency.

**3. Supplementary**

In the first month of placement, I start with testing return merchandise authorization (RMA) from clients. Debugging and testing faulty board provides me with an opportunity to familiarise with Meteor driving systems and different behaviours of print heads. It is considered to be the important preparation step before starting my project.

During the placement, I am not only focused on my background project. Instead, I am quite frequently allocated other tasks with reasonable complexity to gain the insight of what other team members are working on. Currently I am also in a project to develop a testboard which checks whether hardware is manufactured correctly. My responsibility is to design the schematics and PCB. Apart from doing technical work, I had chances to attend conference call as a translator, providing technical support to our clients who are Mandarin speakers. It is a pleasant process to help our engineers communicating with clients and improve the efficiency of conversation.

**4. Summary**

To summarise, the main idea of my project is to include hardware components in regression tests by sending hardware outputs back to PC. This project is expected to be highly beneficial to me. It will practice my technical skills in PCB design, hardware and software development. Also, good communication skill and learning ability are necessary, especially in this technical consulting company.

The placement thus far is very relevant to course content in MEng Electrical and Electronic Engineering. It is always interesting to apply knowledge learned in college to real industry, although industry application is far more complicated than college training. It offers me a great opportunity to gain insight into electronics industry as well as company operation. The last but not least, solving real-world problem and creating values that are visible and beneficial to others is a pleasing process. It always brings me the sense of achievement and reminds me of my role as an engineer.

**5. Appendix**

**5.1 Appendix I. Comparison between using PCC-X and National Instrument Devices**

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| **Approaches** | **Advantages** | **Disadvantages** |
| **PCC-X** | * Flexibility in Function * Convenient to use (replace HDC and testboard to test different print heads) * Low cost * Based on existing project | * Time cost in PCB design and production * Risk brought by bugs in existing projects * Complexity in PC software development (c#) |
| **NI equipments** | * No PCB design required * Lower complexity in software (probably) * High accuracy in analogue signal measurement | * Inconvenience to use (in order to test different HDCs, replacing HDC and changing wiring are inevitable) * High cost in hardware and software purchase * Low flexibility in terms of software function * Time cost of hardware delivery |

A detailed report on evaluating the above two approaches are available for your interest. It is not included in this report due to work limitation.

**5.2 Appendix II. Project Timeline Link**

<https://app.smartsheet.com/b/publish?EQBCT=54ba63bec1864c7388fd33bff1e6b10d>

(Please open with website browser on PC)